

What is Claimed is:

1 1. In a target processor, apparatus for storing a
2 program counter address related to the generation of the a
3 trigger signal, the apparatus comprising:

4 a trigger generation unit coupled to the plurality of
5 event signal generation units, the trigger generation unit
6 responsive to at least one preselected event signal for
7 generating an associated trigger signal, the trigger
8 generating unit also generating a trigger control signal;

9 a register, the register having program counter
10 address related to the trigger signal applied thereto, the
11 register storing the program counter address in response to
12 a control signal generated by the trigger generation unit
13 when the trigger signal is generated; and

14 a delay unit, the delay unit delaying application of
15 the program counter address to the register.

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17 2. The apparatus as recited in claim 1 further
18 comprising a read bus, wherein a second control signal
19 causes the contents of the register to be applied to the
20 read bus.

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22 3. The apparatus as recited in claim 1 wherein a
23 state machine is an event generation unit.

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1 4. The apparatus as recited in claim 1 further
2 comprising:

3 a second register, the second register responsive to
4 the control signal for storing indicia of the events
5 signals.

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7 5. The method of storing a program counter address
8 related to the generation of a trigger signal, the method
9 comprising:

10 generating a event signal for each predetermined
11 event;

12 applying each event signal to a trigger generation
13 unit;

14 when a predetermined event signal or combination of
15 event signals is applied to the trigger generation unit,
16 the trigger generation unit providing a trigger signal and
17 a trigger control signal; and

18 applying the trigger control signal to the storage
19 unit, the storage unit storing the program counter address
20 resulting in the generation of the trigger signal in the
21 storage unit in response to the trigger control signal.

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23 6. The method as recited in claim 5 further
24 comprising the step of delaying the program counter address
25 applied to the storage unit.

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1 7. The method as recited in claim 6 wherein the
2 storage unit is a register.

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4 8. The method as recited in claim 6 wherein a
5 control signal applies the contents of the storage unit to
6 a read bus.

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8 9. The method as recited in claim 4 further
9 comprising storing indicia of each event signal resulting
10 in the trigger signal in a second register in response to
11 the trigger control signals.

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13 10. A target processor comprising: m
14 a state machine, the state machine generating a first
15 event signal in response to a configuration of the target
16 processor;

17 at least one event detection unit, each event
18 detection unit responsive to predetermined configuration of
19 the target processing unit for generating a related event
20 signal;

21 a trigger generation unit, the trigger generation unit
22 generating trigger signal in response to at least one of
23 the first and the related event signals, the trigger unit
24 generating a trigger control signal when the a trigger
25 signal is generated; and

26 a storage unit, the storage unit coupled to the
27 program counter, the program counter applying address

1 signals to the storage unit, the storage unit storing a
2 program counter address in response to the trigger control
3 signal.

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5 11. The target processor as recited in claim 10
6 further comprising a delay line, the delay line delaying
7 the application of the program counter address to the
8 storage unit for a predetermined period of time.

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10 12. The target processor as recited in claim 10
11 further comprising a read bus coupled to the storage unit,
12 the program counter address stored in the storage unit
13 being applied to the read bus in response to a second
14 control signal.

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16 13. The target processing unit as recited in claim 11
17 wherein the storage unit is a register.

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19 14. The target processor as recited in claim 11
20 further comprising a second register, the second storage
21 unit having each event signal applied to at least one
22 associated storage unit position, the storage unit storing
23 applied signals in response to the trigger control signal.